Paragraph **[38]** has been amended as follows:

A2

[38] Furthermore, the present invention provides n+ (or p+) junctions, which are connected to Vcc reference voltage (or ground Vss), additionally between respective active regions each of which includes a limited number of gates (e.g., two gates). Accordingly, the present invention effectively discharges a positive ESD pulse by a parasitic npn bipolar operation occurring between the n+ junctions of the drain region connected to the pad and the additionally-formed active region.